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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/692,687	10/27/2003	Kazuto Usuda	030712-15	2065

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EXAMINER	
ALIA, CURTIS A	

ART UNIT	PAPER NUMBER
2616	

MAIL DATE	DELIVERY MODE
12/11/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/692,687	USUDA ET AL.	
	Examiner	Art Unit	
	Curtis Alia	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 September 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 September 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

Applicant's amendment filed on September 27, 2007 has been entered. Claims 12-15 have been added. Claims 1-15 are still pending in this application, with claims 1 and 10 being independent.

Drawings

1. The drawings were received on September 27, 2007. These drawings are accepted.

Claim Objections

2. Claim 13 is objected to because of the following informalities: Line 3 recites "with the a buffer control circuit." This should be changed to --- with the buffer control circuit --- as in claim 12. Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 2 and 3 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Allowable Subject Matter

5. The indicated allowability of claims 1-9 is withdrawn in view of the newly discovered reference(s) to Jay and Haywood (cited below). Rejections based on the newly cited reference(s) follow.

Claim Rejections - 35 USC § 103

6. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

7. Claims 1-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jay et al. (US 6,400,683) in view of Haywood (US 6,987,775).

For claim 1, Jay discloses a method of controlling a jitter buffer using a FIFO comprising the steps of setting a clock control area (see figure 7, local clock frequency generator) inside the FIFO, raising a clock frequency when the stored packet quantity of the FIFO reaches an upper limit of the clock control area (see column 4, lines 45-47, clock is increased when buffer fills up), lowering the clock frequency when the stored packet quantity of the FIFO reaches a lower limit of the clock control area (see column 4, lines 47-49, clock is decreased when buffer is emptying), and setting the clock control area between the packet add area and the packet delete area (see figure 7, clock area is connected through buffer monitor between both detection circuits on either side of the FIFO buffer).

For claim 1, Jay does not explicitly teach that the method comprises the steps of setting a packet delete area and a packet add area, controlling a stored packet quantity of the FIFO to delete a specified packet when the stored packet quantity exceeds a lower limit of the packet delete area, and to always delete the packets when the stored packet quantity exceeds an upper limit of the packet delete area, controlling the stored packet quantity of the FIFO to add a specified packet when the stored packet quantity falls below an upper limit of the packet add area, and to always add the packets when the stored packet quantity falls below a lower limit of the packet add area. Haywood, from an analogous art, teaches that a FIFO buffer can be

comprised of multiple sections for different functions, such as buffering incoming packets holding monitored packets, and outputting packets to be processed, etc. (see column 2, lines 13-27). As the head buffer fills up, it deletes packets from the head and places them in the tail. As the tail buffer fills up, the overflowed packets are moved to the off-chip memory buffer. Thus, it would have been obvious to a person having ordinary skill in the art at the time of the invention to use a partitioned FIFO buffer with three segments to compartmentalize the packets coming in and going out of the jitter buffer. The FIFO of Haywood can be implemented into the jitter buffer of Jay by using two high speed buffers and a large capacity buffer with a memory controller, as shown in figure 1 of Haywood. The motivation to combine such teachings is that a high data rate can be maintained so that memory read/write speeds do not contribute to the jitter problem introduced by delay variations of the transmission scheme/medium.

For claims 4-6, Jay discloses that the lowering of the clock frequency is linear from the upper limit of the clock control area to the lower limit thereof, and the raising of the clock frequency is linear from the lower limit of the clock control frequency to the upper limit thereof (see column 4, lines 40-49, the clock adjustment method is based on the fill level of the buffer, so the clock frequency is increased in proportion to the fill level of the buffer, and the clock frequency is decreased in proportion to how empty the buffer is).

For claims 7-9, Jay does not explicitly teach that the lowering of the clock frequency is exponential from the upper limit of the clock control area to the lower limit thereof, and the raising of the clock frequency is exponential from the lower limit of the clock control area to the upper limit thereof. However, it would have been common sense to one of ordinary skill in the art that as the buffer gets closer and closer to its maximum capacity, it is in more and more

danger of overflow, thus risking dropped packets. Therefore, to dejitter the packets while still being able to support the flow of incoming packets as well, it would be obvious to increase the rate at which the frequency is being incremented (making the frequency increase in a non-linear, exponential manner). Similarly, as the buffer gets closer and closer to being empty, it is in more and more danger of not having any packets to process (in audio terms, leaving a long silence to the listener), it would be obvious to increase the rate at which the frequency is being decremented (making the frequency decrease in a non-linear, exponential manner).

8. Claims 10 and 12-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jay in view of Haywood and Suzuki et al. (US 2002/0009054).

For claim 10, Jay discloses a device of controlling a jitter buffer comprising a FIFO that configures the jitter buffer (see figure 7, FIFO 700), and a jitter buffer control circuit that includes a buffer accumulation level surveillance that monitors a stored packet quantity accumulated in the FIFO (see figure 7, buffer control circuit comprising comparators 712 and 713, state machine 711), a VCO that supplies to vary a reproduced clock frequency (see figure 7, local clock frequency generator with increment/decrement circuit 706), and a buffer control circuit for controlling the operations of the FIFO and peripheral circuits thereof (see figure 7, state machine), which controls the quantity of packets accumulated in the FIFO to delete packets when the stored packet quantity exceeds a lower limit of the FIFO (see figure 7, detection circuit 701), and controls to add the packets when the stored packet quantity falls below an upper limit of the FIFO (see figure 7, detection circuit 702).

For claim 10, Jay does not explicitly teach that the device further comprises a packet deletion circuit provided on the input side of the FIFO and a packet addition circuit provided on

the output side of the FIFO. Haywood teaches that a FIFO buffer can be comprised of multiple sections for different functions, such as buffering incoming packets holding monitored packets, and outputting packets to be processed, etc. (see column 2, lines 13-27). As the head buffer fills up, it deletes packets from the head and places them in the tail. As the tail buffer fills up, the overflowed packets are moved to the off-chip memory buffer. Thus, it would have been obvious to a person having ordinary skill in the art at the time of the invention to use a partitioned FIFO buffer with three segments to compartmentalize the packets coming in and going out of the jitter buffer. The FIFO of Haywood can be implemented into the jitter buffer of Jay by using two high speed buffers (one added to detection circuit 701 of figure 7 of Jay as a buffer to collect incoming packets, and the other added to detection circuit 702 of figure 7 of Jay as a buffer to output the packets to be processed) with a FIFO buffer, as shown in figure 1 of Haywood. The motivation to combine such teachings is that a high data rate can be maintained so that memory read/write speeds do not contribute to the jitter problem introduced by delay variations of the transmission scheme/medium.

For claim 10, Jay and Haywood do not explicitly teach that the jitter buffer controller further comprises a decoder that accepts the packets outputted from the packet addition circuit and decodes frames of the packets based on the clock frequency supplied from the VCO. Suzuki, from the same field of endeavor teaches that a jitter buffer controller receiving voice packets comprises a voice decoder (see figure 2, voice decoder 110 connected to delay unit 103 with input clock frequency from internal clock generator 107). Thus, it would have been obvious to a person having ordinary skill in the art at the time of the invention that the audio packets being processed through the jitter buffer of Jay would be decoded into an audible analog

signal to be output to the user. The motivation to combine such teachings is that the packets are only useful to the user if they are properly decoded (in this case, a voice decoder is needed to decode the packets into audible signals outputted to a speaker).

For claim 12, Jay and Haywood teach that the jitter buffer control circuit is in direct communication with the packet deletion circuit and the packet addition circuit. As stated in the rejection of claim 10, Jay's detection circuits can be modified to include buffers for add and delete circuits, which are directly connected to the jitter buffer control circuit (see figure 7 of Jay, detection circuits 701 and 702 are connected to the buffer control circuits through the up/down counter 703)

For claim 13, Jay and Haywood teach that the packet deletion circuit and the packet addition circuit are in direct communication with the buffer control circuit of the jitter buffer control circuit. As stated in the rejection for claim 12, Jay's detection circuits combined with Haywood's buffers to make packet addition and deletion circuits are connected to the buffer control circuits of the jitter buffer control circuit through the up/down counter 703.

For claim 14, Jay teaches that the jitter buffer control circuit is in direct communication with the jitter buffer. In figure 7, the buffer limits B_{min} and B_{max} are monitored by the buffer limit comparators 712 and 713, thus showing a direct connection between the jitter buffer and the jitter buffer control circuit.

For claim 15, Jay teaches that the jitter buffer is in direct communication with a buffer monitoring portion of the jitter buffer circuit. In figure 7, the buffer limits B_{min} and B_{max} are monitored by the buffer limit comparators 712 and 713 (buffer monitoring portion), thus

showing a direct connection between the buffer monitoring portion and the jitter buffer control circuit.

9. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jay in view of Suzuki as applied to claim 10 above, and further in view of Oltean (US 6,044,113).

For claim 11, Jay and Suzuki fail to teach that the jitter buffer controller can use a pulse width modulator as a replacement for the VCO. Oltean, from an analogous art, teaches that a pulse width modulation circuit can produce a clock signal (see abstract). Thus, it would have been obvious to a person having ordinary skill in the art at the time of the invention to use any type of clock generating circuit, including a pulse width modulation circuit, to generate a clock frequency used in a jitter buffer controller. This can be implemented into the jitter buffer controller by replacing the traditional VCO with the pulse width modulator circuit as taught by Oltean. The motivation to combine such teachings is that the highs and lows of the clock signals can be varied independently.

Response to Arguments

10. Applicant's arguments with respect to claims 10 and 11 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

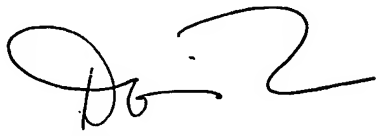
11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Curtis Alia whose telephone number is (571) 270-3116. The examiner can normally be reached on Monday through Friday, 8am-5pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Doris To can be reached on (571) 272-7629. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

CAA



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